Specification Q5B

ASIC for RFID

Product : Multifunctional Read/Write Identification ASIC

Prod. No. : Q5

Issue : 2 **Date :** November 11th, 2001

Revision : B **Date :** November 11th, 2001

	FUNCTION	NAME	SIGNATURE	DATE
APPROVED BY	R&D Manager	K. Fietze		
APPROVED BY	R&D Manager	U. Furter		
APPROVED BY	Quality Manager	I. Ceausoglu		
APPROVED BY	Plant Manager	M. Ruokanen		

CHANGE RECORD

REVISION	DATE	PAGES	MODIFICATIONS
A	March 14th, 2001		First approved version
D	November 11th, 2001		Complete redesign

DISTRIBUTION LIST

DEPARTMENT / NAME			QUANTITY
SOKYMAT			
Management	:	M. Ruokanen	1
Quality	:	I. Ceausoglu	1
Product Development	:	U. Furter	1
Product Management	:	P. Blanc	1
Product Management	:	D. Cardinaux	1
Product Management	:	L. Schwarz	1
Production	:	D. Bigler	1

CONTENT

1. GENERAL DESCRIPTION

The **Q5B** is a contact-less R/W–**ide**ntification IC for applications in the 125–kHz frequency range. A single coil, connected to the chip, serves as the IC's power supply and bidirectional communication interface. Antenna and chip together form a transponder or tag.
The on–chip 330–bit EEPROM (10 blocks 32 data bits) can be read and written blockwise from a base station. One block is reserved for setting the operation modes of the **Q5B**. Another block may contain a password to prevent unauthorized writing.
Data is transmitted from the **Q5B** (uplink) using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1/ Coil 2. The IC receives and decodes 100% amplitude modulated (OOK) pulse–width encoded bit streams from the base station.

2. FEATURES

- Contact-less power supply
- Contact-less read/write data transmission
- Radio frequency f_{RF} from 100 to 150 kHz
- Integrated capacitor 80, 130 or 210 pF
- 7 x 32 bit EEPROM data memory including 32 bit password memory
- Separate 64–bit memory for traceability data
- 32 bit configuration register in EEPROM to set up:

Data bit rate:
- RF/2 to RF/128, binary selectable

Modulation type:
- FSK, Manchester, Biphase, PSK, NRZ

Other options:
- Password mode
- Max block feature
- Answer–On–Request (AOR) mode
- Inverse data output
- Direct access mode
- Disable test mode access
- Fast write method (~ 5 kbps vs. ~ 2 kbps)
- Write protection (through lock–bit per block)
- Sequence terminator

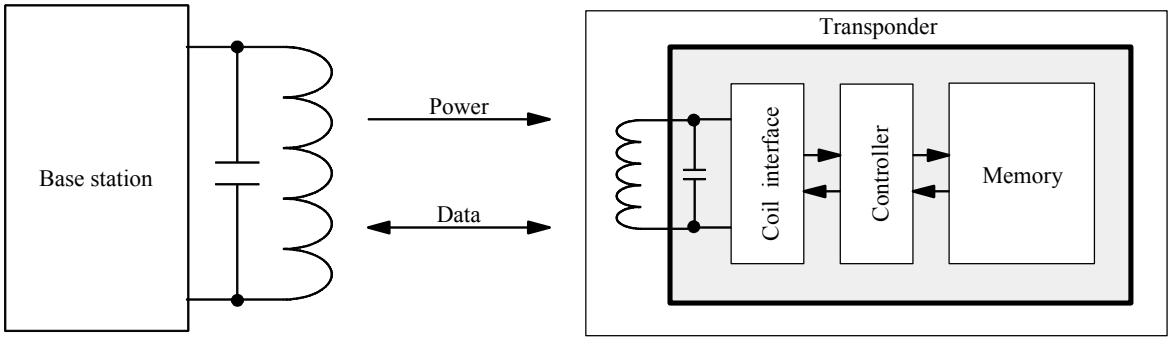


Figure 1. RFID system using Q5B

3. Q5B BUILDING BLOCKS

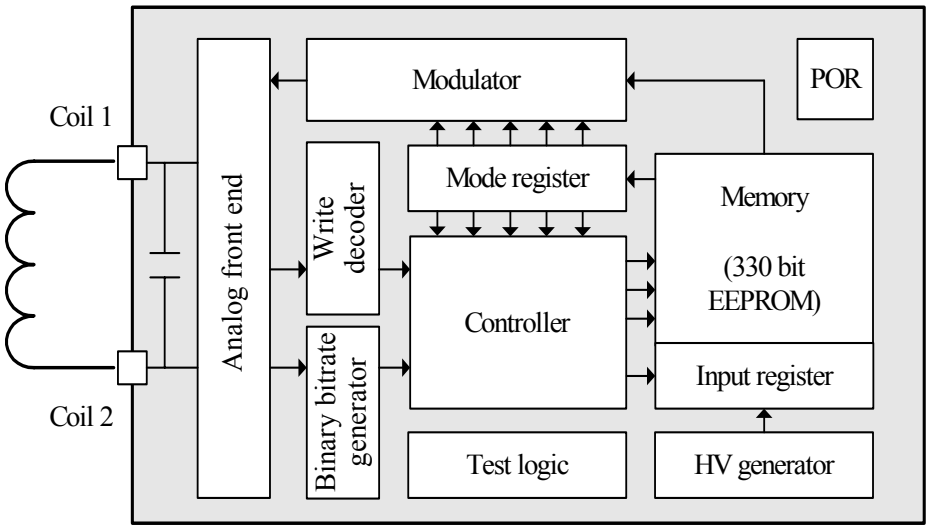


Figure 2. Block diagram Q5B

3.1. Analogous Front End (AFE)

The AFE includes all circuits, which are directly connected to the coil. It generates the IC's power supply and handles the bi–directional data communication with the reader unit. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between COIL1 / COIL2 for data transmission from Q5B to the reader (uplink mode)
- Field gap detector for data transmission from the base station to the Q5B (downlink mode)
- ESD protection circuitry

3.2. Data Bit Rate Generator

The data rate is binary programmable to operate at any bit rate between RF/2 and RF/128. If the "page select" bit is set, the data encoding and bit rate is fixed to Manchester RF/64.

3.3. Write Decoder

This function decodes the write gaps and verifies the validity of the data.

3.4. HV Generator

The on–chip charge pump generates the high voltage required for programming of the EEPROM.

3.5. Power–On Reset (POR)

This circuit delays the IDIC functionality until an acceptable voltage threshold has been reached.

3.6. DC Supply

Power is externally supplied to the **Q5B** via the coil connections. The IC rectifies and regulates this RF source and uses it to generate it's supply voltage.

3.7. Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

3.8. Control Logic Module

The control logic has the following functions:

- Load mode register with mode data from EEPROM block 0 after power–on and also during reading
- Control memory access (read, write)
- Handles write data transmission and write error modes
- The first two bit of the write data stream are the op-code, e.g. standard write or test mode.
- In password mode, the 32 bit received after the op-code are compared with the password stored in block 7.

3.9. Mode (Configuration) Register

This register stores the mode data from the EEPROM configuration block. It is continually refreshed at the start of every block read.

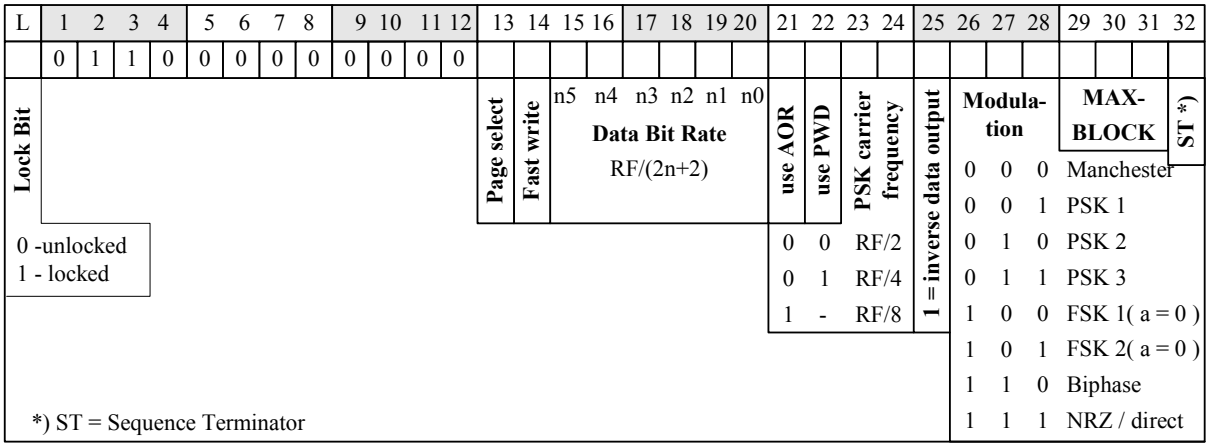


Figure 3. Q5B configuration block 0 bit mapping

3.10. Modulator

The modulator consists of data encoders for the following basic types of modulation:

Table 1

Mode	Direct Data Output	Inverse Data Output
FSK 1a [1)]	'0' = f1 = rf/8; '1'= f2 = rf/5	'0' = f2 = rf/5; '1' = f1 = rf/8
FSK 2a [1)]	'0' = f1 = rf/8; '1'= f2 = rf/10	'0' = f2 = rf/10; '1' = f1 = rf/8
PSK1 [2)]	Phase change when input changes	Phase change when input changes
PSK2 [2)]	Phase change on bit clock if input high	Phase change on bit clock if input low
PSK3 [2)]	Phase change on rising edge of input	Phase change on falling edge of input
Manchester	'0' = falling edge, '1'= rising edge on mid–bit	'1' = falling edge, '0'= rising edge on mid–bit
Biphase	'1' creates an additional mid–bit change	'0' creates an additional mid–bit change
NRZ	'1'= damping on, '0'= damping off	'0'= damping on, '1'= damping off

Notes: 1) A common multiple of bit rate and FSK frequencies is recommended.
2) The PSK carrier frequency and bit rate should fulfil the Nyquist criterion.
3) When using PSK-mode the data rate must be a multiple of the sub carrier frequency.

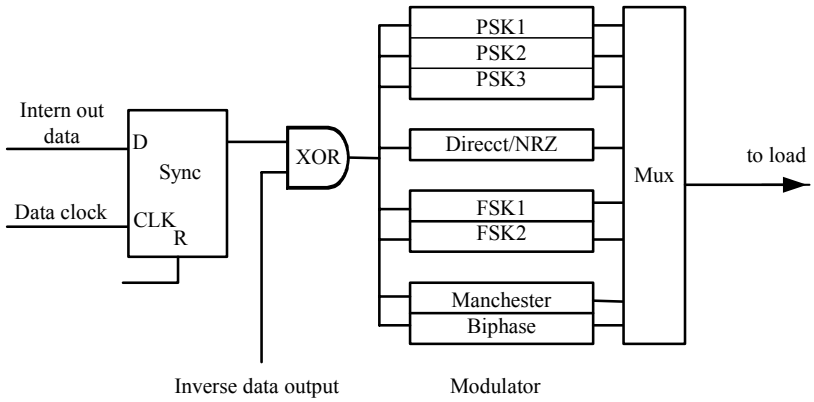


Figure 4. Data encoder for inverse data output

3.11. Memory

The memory is a 330 bit EEPROM, which is arranged in 10 blocks of 33 bit each. All 33 bits of a block - including the lock bit - are programmed simultaneously.

Block 0 of page 0 contains the mode-/configuration data, which is not transmitted during normal read operation.

Block 7 of page 0 may be used as a write protection password.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lock bit itself) is not re-programmable through the RF field again.

Block 1 and 2 of page 1 are addressed if the “page select” in the mode register is set or the op-code ’11’ is issued.

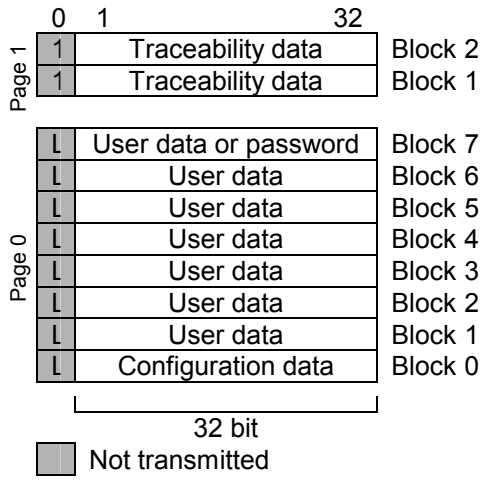


Figure 5. Memory map

3.12. Page 1 - Traceability Data Structure

Block 1 and 2 of page 1 contain the traceability data formatted in the following way.
The header is composed of the first 9 bits, which are all set to ’1’. Due to the data and parity organisation, this sequence cannot be reproduced in the data string. The header is followed by 10 groups of 4 data bits and an even row parity bit per digit. The 11th digit consists of 4 even column parity bits followed by a stop bit which is fixed to ’0’. The 40 bit (D00 to D93) encode the following information.

- D00 to D01 IC revision
- D02 to D03 Lot ID char, e.g.: ’Z’ = ’00’, ’Y’ = ’01’
- D10 to D50 17 bit binary lot ID ’00001’ to ’99999’
- D51 to D61 5 bit binary wafer no.: ’1’ to ’25’
- D62 to D93 14 bit sequential die per wafer no.:’1’ to ’16000’

Block 1 starts with the header and including bit D42 whereas block 2 contains bit D43 up to the stop bit (’0’). The traceability data as encoded in blocks 1 and 2 of page 1 is programmed and write protected (locked) during production test.
The 64-bit data string of page 1 is transmitted respectively by the Q5B until power goes off, if the “page select” bit in the configuration register (block 0, bit 13) is set.
The Manchester encoded is ASK modulated with a fixed data rate of RF/64, independent from any other mode register settings.
If the “page select” bit is reset, the traceability data stored in page 1 may be accessed by a reader/interrogator using a short ’11’ op-code command. Any new command or gap will stop the page 1 read–out and the tag may return to regular read mode.

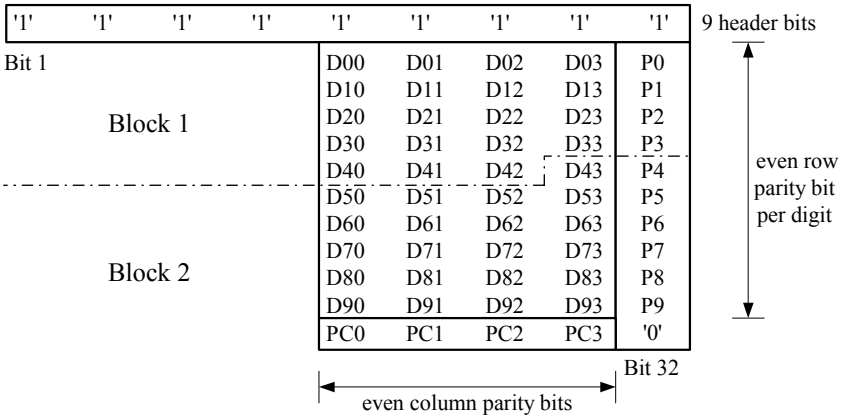


Figure 6. Traceability data structure

4. OPERATING THE Q5B

4.1. Initialisation

Power–On–Reset circuit (POR) remains active until an adequate voltage threshold has been reached. This in turn triggers the default start-up delay sequence. During this period of about 128 field clock cycles (FC) the Q5B is initialised with the configuration data stored in EEPROM block 0. During initialisation of the configuration block, modulation is switched off. Any field gap during the initialization time of 3 ms will restart the complete sequence.
After this initialization time the Q5B enters regular read mode and modulation starts automatically using the parameters defined in the configuration block.

4.2. Uplink Mode

Under normal operation, the data stored within the EEPROM is cycled and the Coil 1, Coil 2 terminals are load modulated. This backscatter modulation can be detected at the reader module.

4.3. Data Encoding

Every time entering regular read mode, the first bit transmitted is a logical ’0’. The data stream starts with block 1, bit 1, continues through MAXBLK, bit 32, and cycles continuously if in regular read mode.

4.4. Direct Access Command

With the direct access command only the addressed block is repetitively read, this mode is called block–read mode. Direct access is entered by transmitting the access op-code (‘10’), a single ‘0’ bit and the requested 3-bit block address, if the tag is in normal mode.
In password mode (use PWD set), the direct access to a single block needs the valid 32–bit password to be transmitted after the access op-code (’10’) whereas a ’0’ bit and the 3–bit block address follow afterwards. In case the transmitted password does not match with the contents of block 7, the Q5B tag returns to the regular read mode immediately.

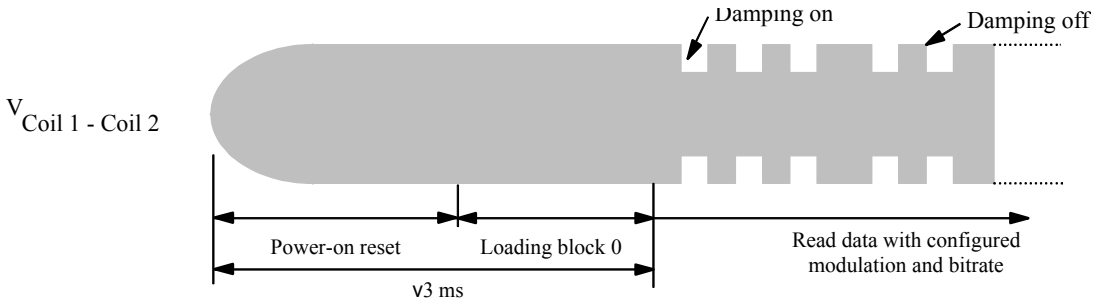


Figure 7. Voltage at Coil1 / Coil2 after power-on

4.5. MaxBlock Feature = No of Readable Blocks

Data from the memory is serially transmitted, starting with block 1, bit 1, up to the last block (e.g. 7), bit 32. The mode parameter field MAXBLK in EEPROM block 0 defines the last block, which will be read. When the MAXBLK address has been read, data transmission restarts with block 1, bit 1.
The user may limit the cyclic data stream in regular read mode by setting the MAXBLK between 0 and 7 (representing each of the 8 data blocks of the page 0). If set to 7, blocks 1 through 7 can be read. If set to 1, only block 1 is transmitted continuously. If set to 0, the contents of the configuration block (normally not transmitted) can be read. In the case of MAXBLK = 0 or 1 regular read mode is not distinguishable from block read mode.

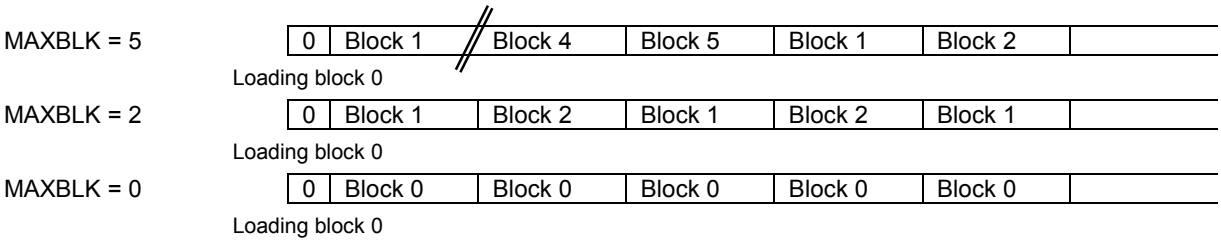


Figure 8. Examples of MAXBLK features

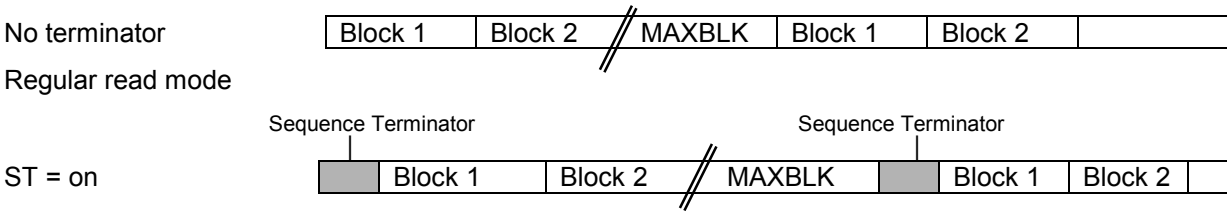


Figure 9. Read data stream with sequence terminator

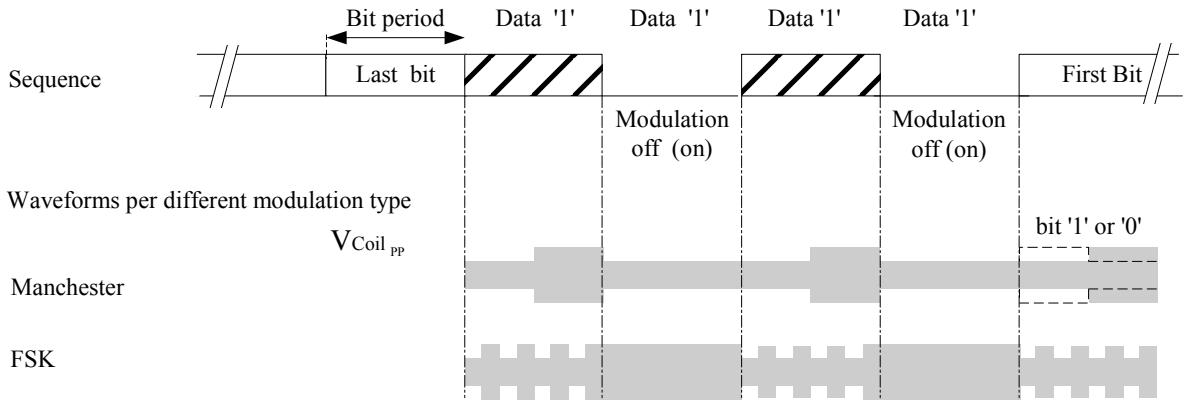


Figure 10. e5550–compatible sequence terminator waveforms

4.6. Sequence Terminator

The sequence terminator ST is a special damping pattern, which follows the last block and may be used to synchronize the reader. The e5550–compatible sequence terminator which is valid for Manchester (ASK) and FSK modulation consists of 4 bit periods with underlaying data values of '1'. During the second and fourth bit period modulation is switched off (Manchester encoding - switched on).
The sequence terminator is enabled by setting of mode bit 32 (ST = '1').
In the regular read mode the sequence terminator is inserted at the start of each MAXBLK–limited read data stream.
In block–read mode - after any block–write or direct–access command - or if MAXBLK was set to '0' or '1', the sequence terminator is inserted before the transmission of the selected block.

4.7. Downlink Mode

Data is written to the Q5B by interrupting the RF field with short gaps in accordance with a predefined scheme. If the data transfer was successful, the content is programmed into the EEPROM memory. An optional block-write protect bit can be set.

4.8. Start Gap

The initial gap is referred to as the start gap. This triggers the downlink mode. During the downlink mode, the receive damping is permanently enabled to ease gap detection. The start gap needs to be longer than subsequent gaps in order to be detected reliably.
A start gap will be accepted at any time after the mode register has been loaded (≥ 3 ms).

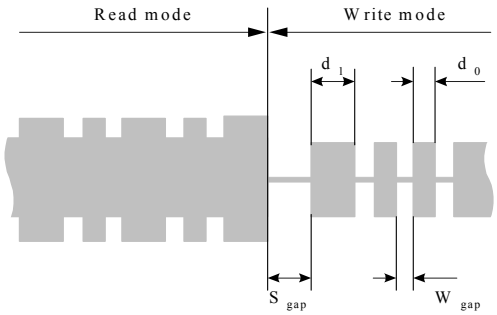


Figure 11. Start of writing

4.9. Write Decoder

The duration of the gaps is usually in the range of 14 field clocks. In normal write mode the time between two gaps is nominally 24 field clocks for a "0" and 54 field clocks for a "1". When there is no gap for more than 64 field clocks after a previous gap, the Q5B exits the downlink mode; it starts with programming if the correct number of bits were received. If there is a gap failure – the Q5B does not start programming, instead it will enter regular read mode (except if in AOR mode).
In the optional fast write mode the time between two gaps is nominally 12 field clocks for a "0" and 28 field clocks for a "1". When there is no gap for more than 32 field clocks after a previous gap, the Q5B will exit the downlink mode.

4.10. Writing Data

The Q5B always expects to receive a dual bit write op-code first. Writing has to follow these rules:

- Standard writing needs the op-code, the lock bit, the 32 data bits and the 3 bit address (38 bit in total).
- Writing with usePWD set requires a valid 32 bit password between op-code and the address/data bits.
- In AOR mode with usePWD set op-code and a valid password are necessary to enable modulation.

Note: Data bits are read in the same order as written.

Table 2. Write data decoding schemes

Parameters	Remark	Symbol	Min.	Typ.	Max.	Unit	Test
Start gap		S_{gap}	10		50	FC	Q
Write gap	Normal write mode	Wn_{gap}	8		50	FC	Q
	Fast write mode	Wf_{gap}	8		25 (50)	FC	Q
Write data in normal mode	'0' data	d_0	16		31	FC	Q
	'1' data	d_1	48		63	FC	Q
Write data in fast mode	'0' data	d_0	8		15	FC	Q
	'1' data	d_1	24		31	FC	Q

4.11. Op-codes

If the transmitted command sequence is invalid, the Q5B starts uplink mode in regular read mode after the last gap.

- The RESET op-code ”00” precedes a ’soft’ reset cycle (which is normally used for test purposes only)
- The standard op-code ”10” precedes all block write and direct access operations to page 0.
- Receiving the op-code “11” results in the transmission of the Manchester encoded 64–bit traceability data of page 1 with the data rate of RF/64.
- An optional modulation defeat switch op-code ”00011” turns the tag into quiet state.

4.12. Password

When password mode is activated (usePWD = 1), the first 32 bit after the op-code are regarded as the password. They are compared bit–by–bit with the contents of block 7, starting at bit 1. If the comparison fails, the Q5B will not program the memory, but restart in regular read mode once the last gap has been received.

Notes

- If the usePWD bit is zero, the Q5B accepts any bit stream containing 32 data bit in place of a password and will enter programming mode.
- In password mode, MAXBLK should be set to a value below 7 to prevent the password from being transmitted by the Q5B.

Every transmission of the two op-code bits, 32 bit for a password, plus ’0’ and 3 address bits (= 38 bit) needs about 10 ms. Testing all 232 possible combinations (about 4.3 billion) takes over two years using the normal write method.

4.13. Answer–On–Request (AOR) Mode

When the AOR bit is set, the Q5B does not start modulation in the read mode after loading of configuration block 0. The IC waits for a valid AOR data stream (“wake-up command”) from the reader before modulation is enabled. The wake-up command consists of the op-code (’10‘) followed by a valid password. The Q5B will remain active until the RF field is turned off or a new command with a different password is received.

Table 3. Q5B - Modes of operation

PWD	AOR	Behaviour of Tag after Reset Command or POR	De–activate Function
1	1	Answer–on–request (AOR) mode: • Modulation starts after wake-up with a matching PWD • Programming needs valid PWD	Command with non-matching password de-activates the selected tag
1	0	Password mode: • Modulation starts after reset • Programming and direct access needs valid PWD	Modulation defeat command disables all tags in the field
0	-	Plain/Normal mode: • Modulation starts after reset • Programming and direct access without password	

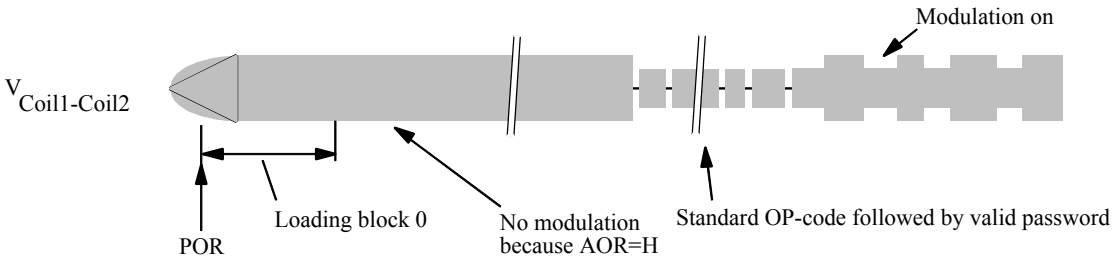


Figure 12. Answer–on–request (AOR) mode

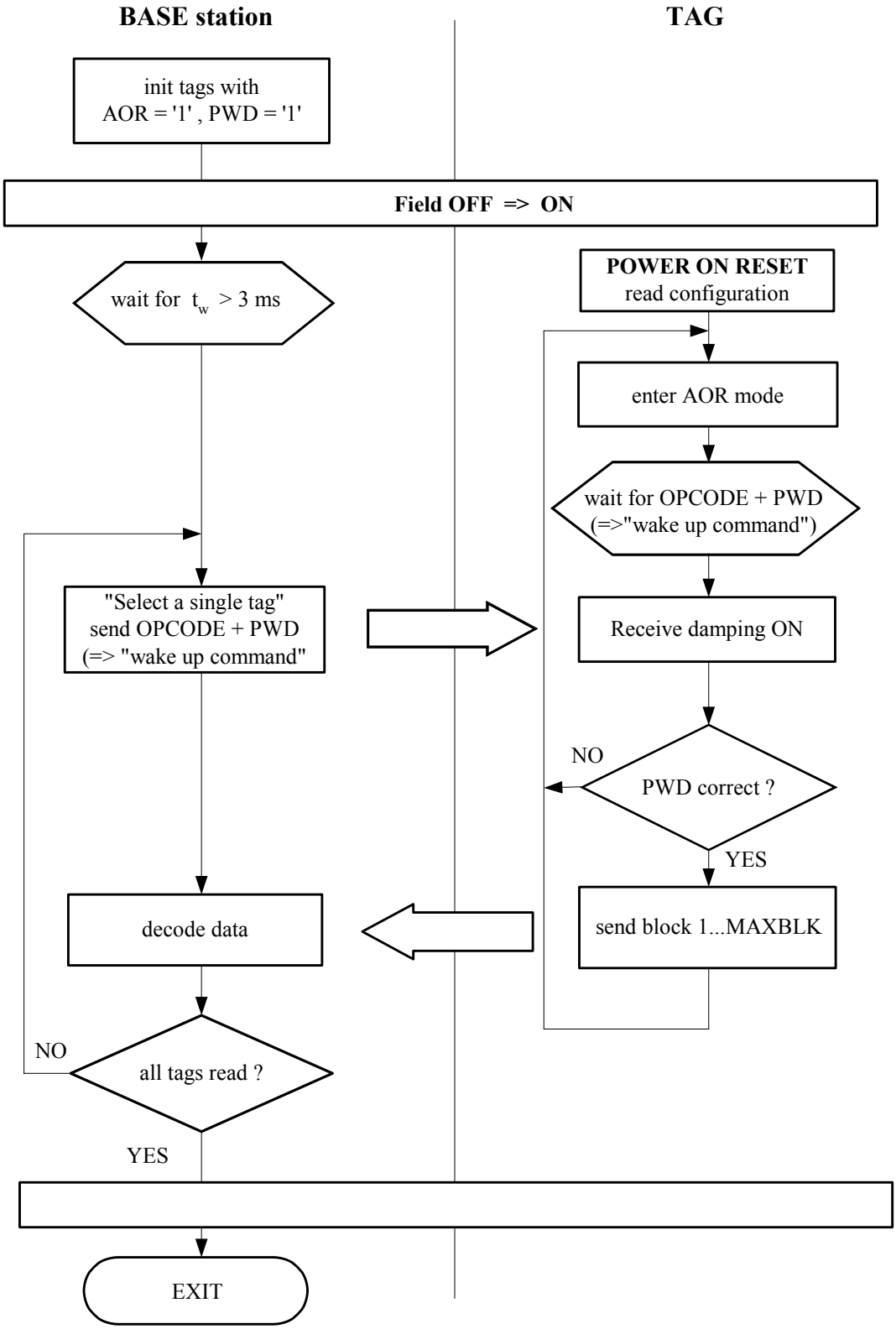


Figure 13. Answer–on–request procedure

4.14. Programming

When all necessary information has been transmitted to the Q5B, programming may proceed. There is a clock delay between the end of the write data stream and the start of programming.
Typical programming time is 5.7 ms. This cycle includes a data verification read to grant secure and correct programming. After programming is done, the Q5B enters block–read mode, with the block just programmed.

Valid bit counts are:

- Password write 70 bit (usePWD = 1)
- Standard write 38 bit (usePWD = 0)
- AOR wake up 34 bit (usePWD = 1)
- Direct access 38 bit (usePWD = 1)
- Direct access 6 bit (usePWD = 0)
- Modulation defeat 5 bit
- 64–bit page 1 read 2 bit
- Reset command 2 bit

4.15. Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

4.16. Errors During Writing

The following detectable errors could occur during writing data into the Q5B:

- Wrong number of field clocks between two gaps (i.e. not a valid ”1” or ”0” pulse with bit stream).
- Password mode is activated and the password does not match the contents of block 7.
- The number of bits received in the command sequence is incorrect.

If any of these conditions are detected, the Q5B enters regular read mode, except AOR is active.

4.17. Errors During Programming

If writing was successful, the following error could prevent programming:

- The lock bit of the addressed block is set.

In this case, programming mode will not be entered. The Q5B reverts to uplink mode, continuously transmitting the currently addressed block (block–read mode).

- Data verification error

In this case, programming has failed and the Q5B enters modulation defeat until a new command is transmitted or the IC enters power–on reset.

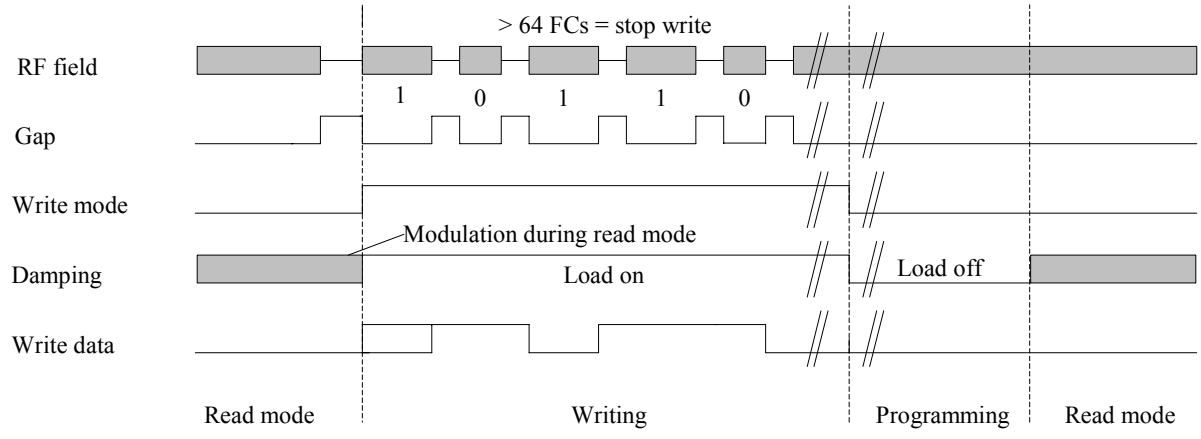


Figure 14. Signals during writing

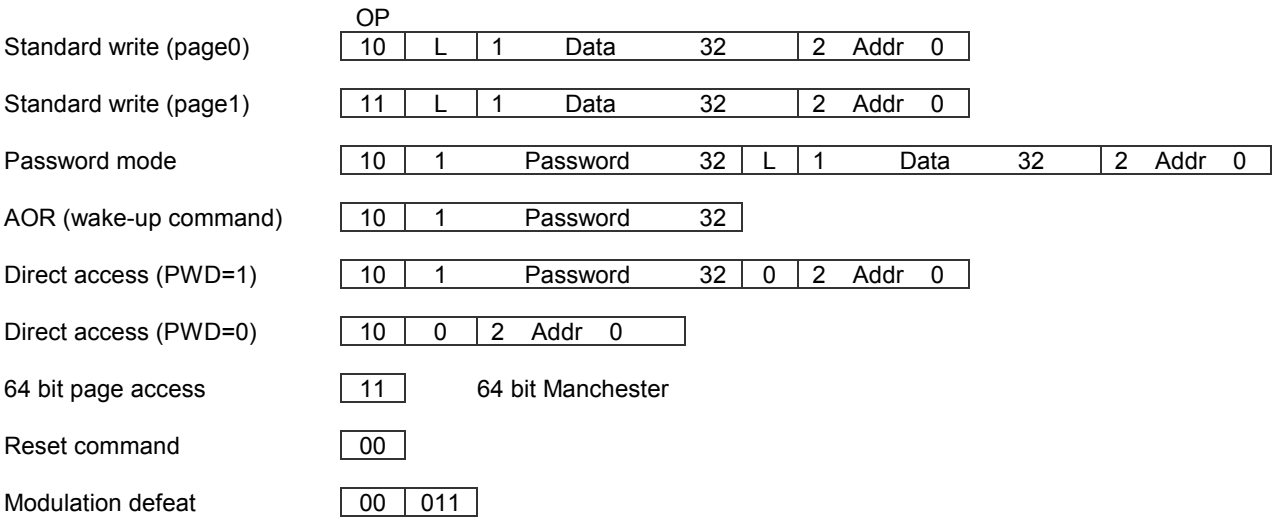


Figure 15. Q5B command formats

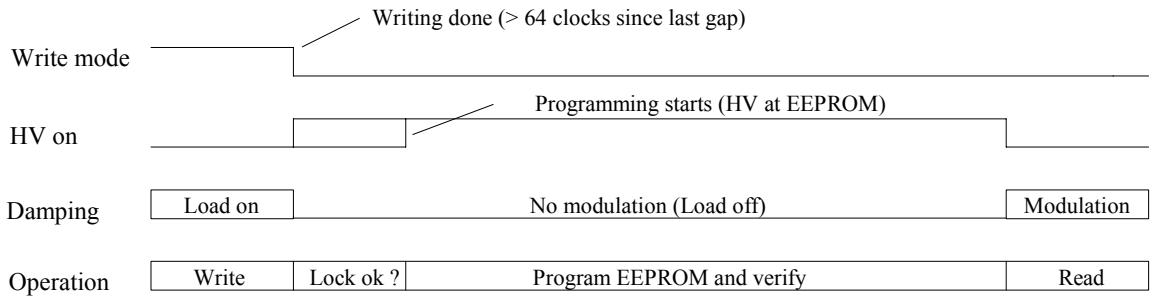


Figure 16. Programming

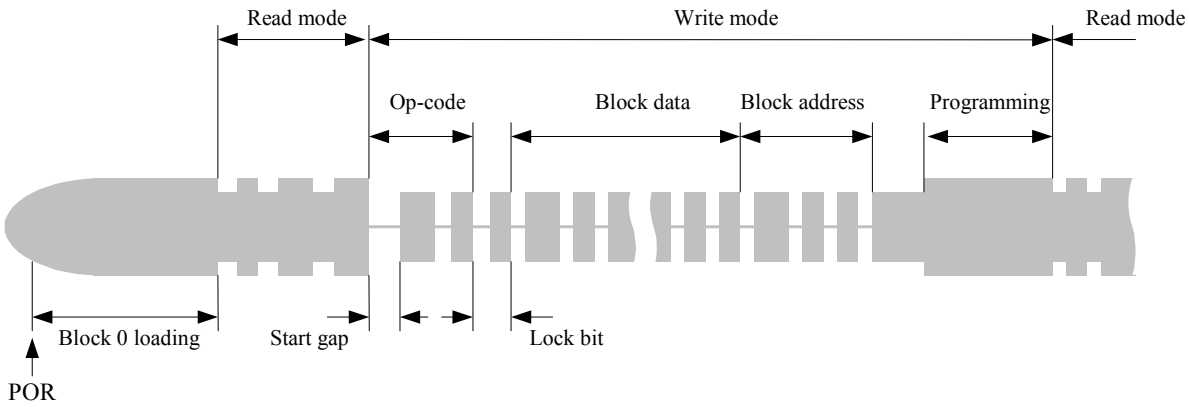


Figure 17. Complete writing sequence

4.18. Power On Reset

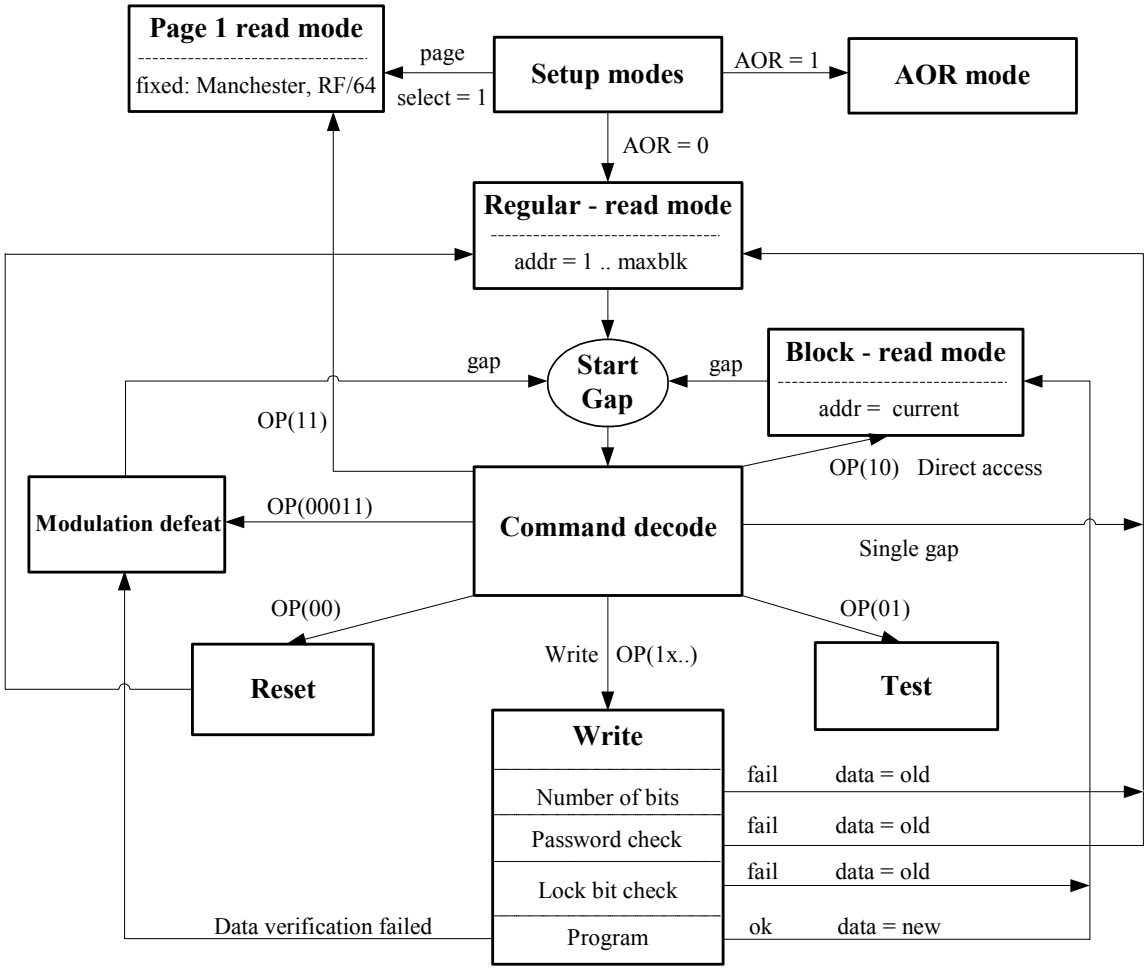


Figure 18. Q5B functional diagram

5. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Electrostatic discharge maximum to MIL–Standard 883 C method 3015	V_{max}	4,000	V
Operating ambient temperature range	T_{amb}	-40 to +85	°C
Storage temperature range (data retention reduced)	T_{stg}	-40 to +150	°C

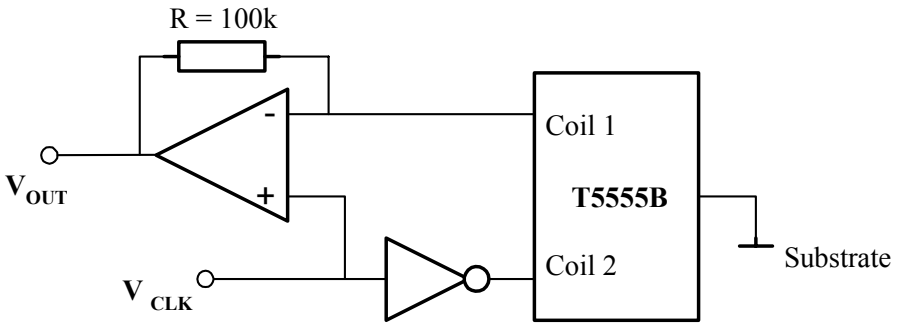
6. OPERATING CHARACTERISTICS

T_{amb} = +25 °C; f_{coil} = 125 kHz; unless otherwise specified
T: tested directly or indirectly during production
Q: guaranteed based on initial product qualification data

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	Test
RF frequency range		f_{RF}	100	125	150	kHz	
Coil voltage (AC supply)	POR threshold (50 mV hysteresis)	$V_{coil\ pp}$	3.2	3.6	4.0	V	Q
	Read mode and write command [2]		6		V_{clamp}	V	Q
	Program EEPROM [2]		8		V_{clamp}	V	Q
Startup time	$V_{coil\ pp}$ = 6 V	$t_{startup}$		2.5	3	ms	Q
Programming time	From last command gap to re–enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
Programming cycles	Erase all / Write all [1]	n_{cycle}	100,000			Cycles	Q
Data retention	Top = 55 °C [1]	$t_{retention}$	10	20	50	Years	

Notes:

1. Since the assembly process influences EEPROM performance, SOKYMAT confirms these parameters for all SOKYMAT products.
2. Current into COIL1/COIL2 is limited to 10 mA.
3. The tolerance of the capacitor is ± 10% @ 3s over whole production. The capacitor tolerance is ± 3% @ 3σ on a wafer basis.
4. @ V_{coil} = 5 V: EEPROM programmed to 00 ... 000 (erase all) in modulation defeat.
5.



$$I_{DD} = (V_{OUTmax} - V_{CLK}) / R$$

Figure 19. Measurement set-up for I_{DD}

6.

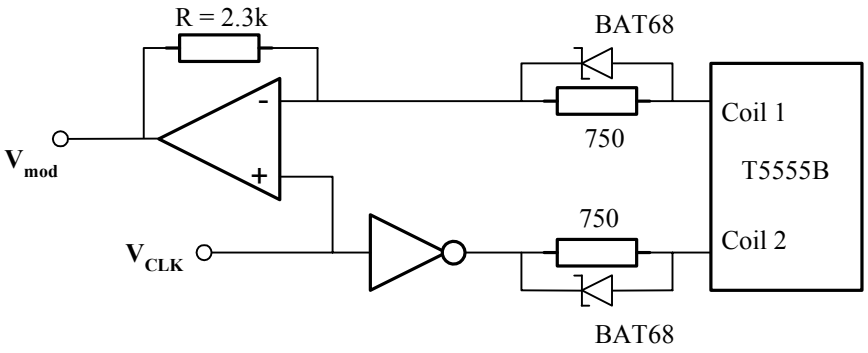


Figure 20. Measurement set-up for V_{mod}

7. Extrapolated from single cell measurements and 150 °C data retention tests.

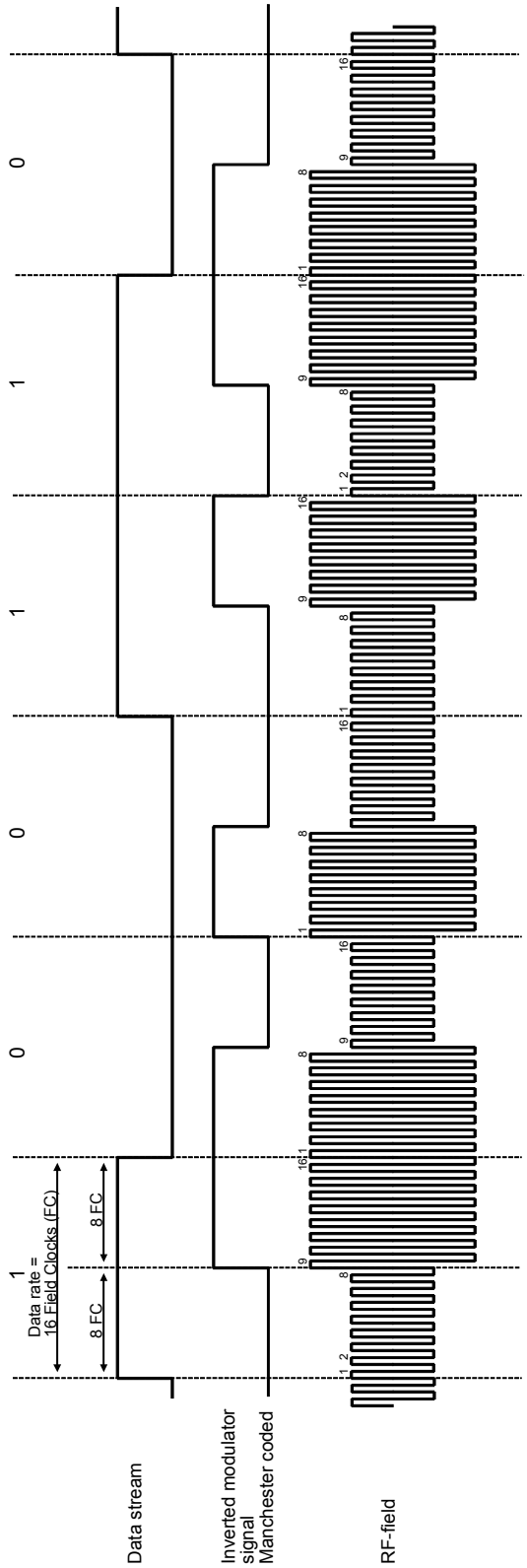


Figure 21. Example of Manchester coding with data rate RF/16

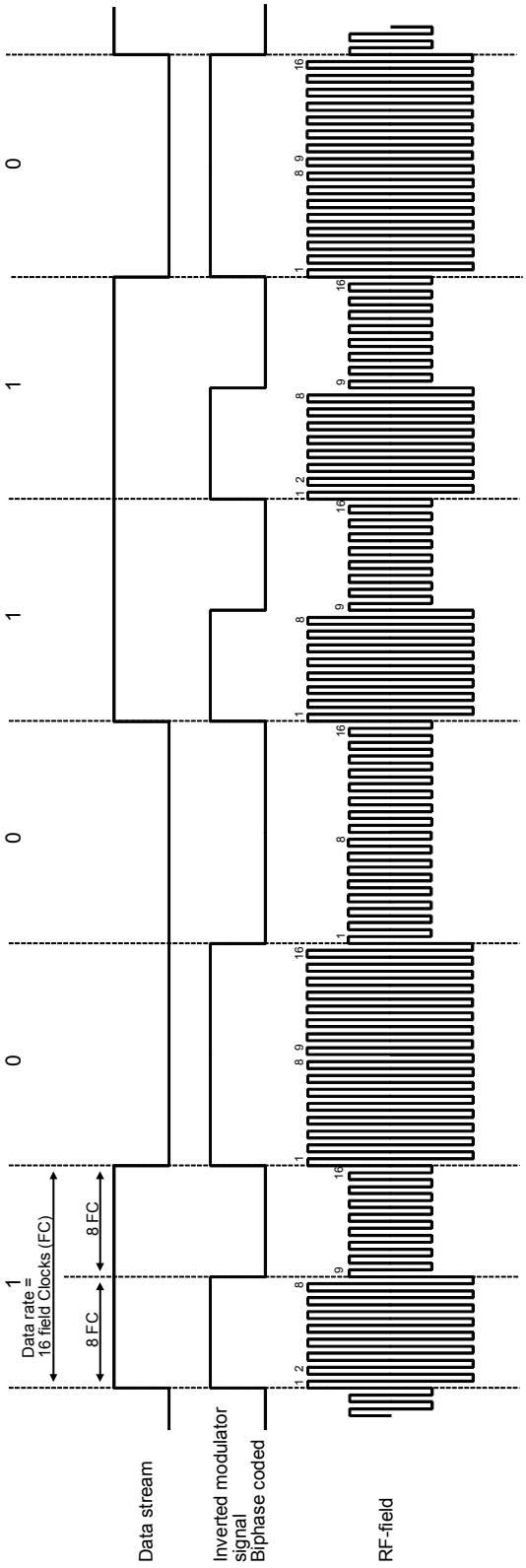


Figure 22. Example of Biphase coding with data rate RF/16

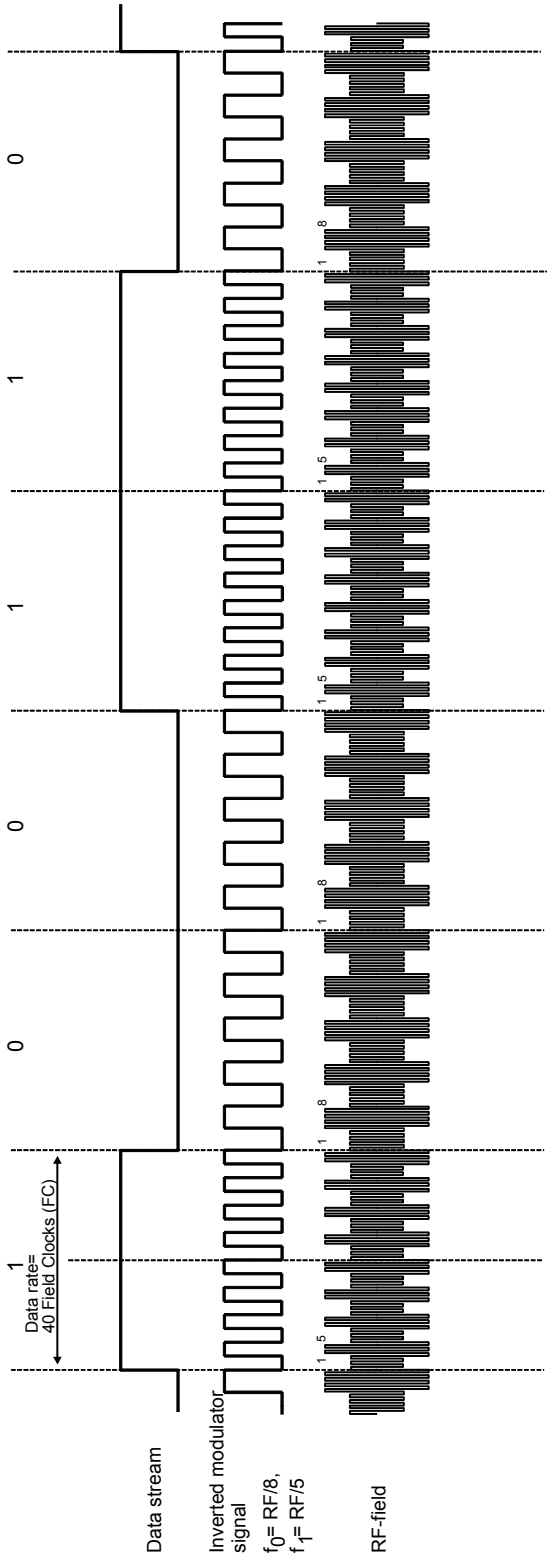


Figure 23. Example of FSK coding with data rate RF/40, subcarrier f_0 = RF/8, f_1 = RF/5

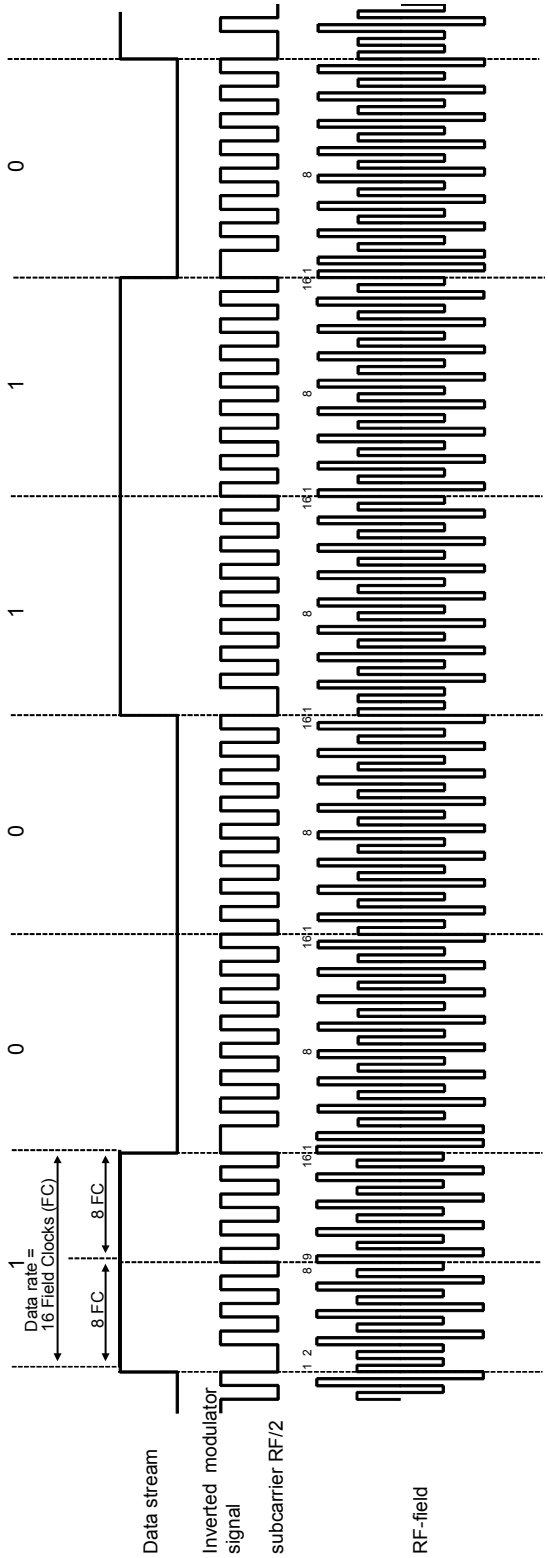


Figure 24. Example of PSK1 coding with data rate RF/16

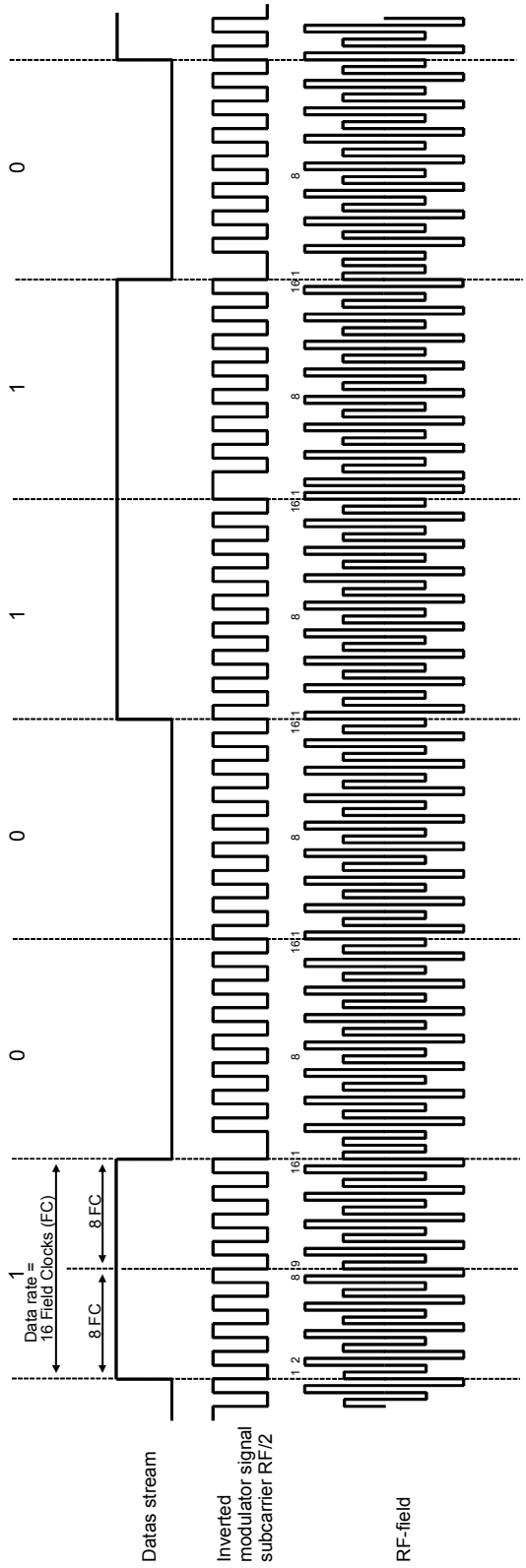


Figure 25. Example of PSK2 coding with data rate RF/16

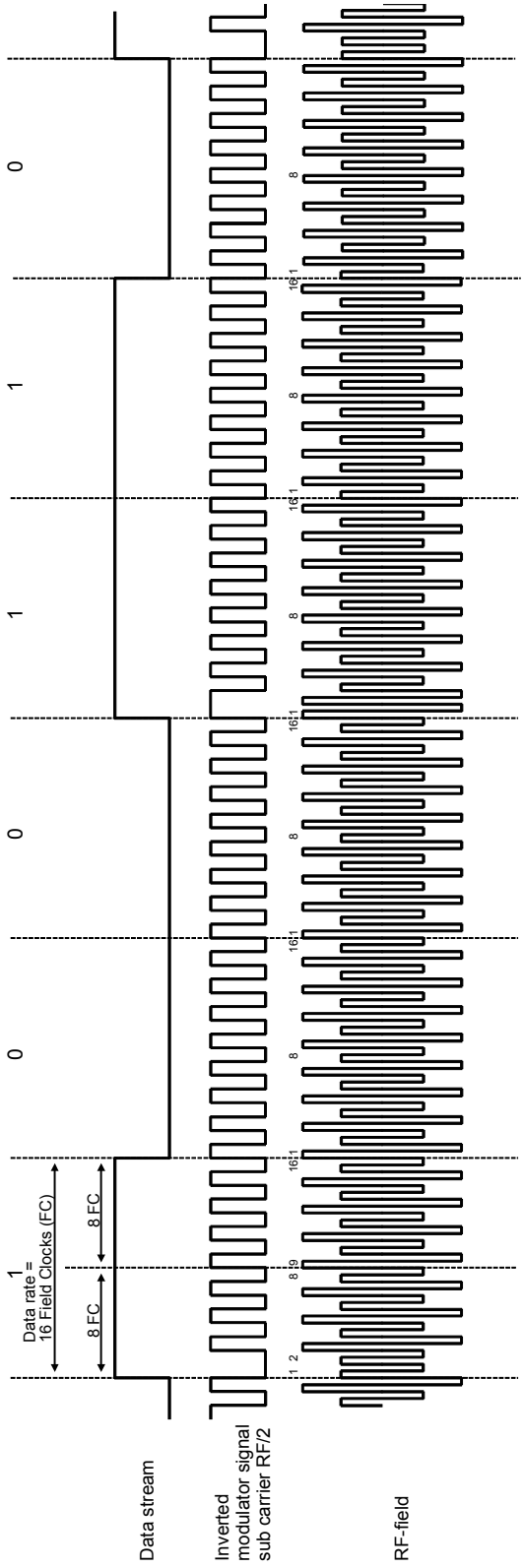


Figure 26. Example of PSK3 coding with data rate RF/16

We reserve the right to make changes to improve technical design and may do so without further notice – in case of customer–specific products only where such changes do not cause substantial changes in customer–specific specifications.

Parameters can vary in different applications. The customer must validate all operating parameters for each customer application. Should the buyer use SOKYMAT products for any unintended or unauthorized application, the buyer shall indemnify SOKYMAT against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

SOKYMAT S.A., Zone industrielle, CH-1614 Granges (Veveyse), Switzerland
Telephone: +41 (021) 9080 110, Fax: +41 (021) 9080 105