Read Only Contactless Identification Device

Features

- 64 bit memory array laser programmable
- Several options of data rate and coding available
- On chip resonance capacitor
- On chip supply buffer capacitor
- On chip voltage limiter
- Full wave rectifier on chip
- Large modulation depth due to a low impedance modulation device
- Operating frequency 100 - 150 kHz
- Very small chip size convenient for implantation
- Very low power consumption

Description

The H4102 is a CMOS integrated circuit for use in electronic Read Only RF Transponders. The circuit is powered by an external coil placed in an electromagnetic field, and gets its master clock from the same field via one of the coil terminals. By turning on and off the modulation current, the chip will send back the 64 bits of information contained in a factor programmed memory array.
The programming of the chip is performed by laser fusing of polysilicon links in order to store a unique code on each chip.
The H4102 has several metal options which are used to define the code type and data rate. Data rates of 64, 32 and 16 periods of carrier frequency per data bit are available. Data can be coded as Manchester, Biphase or PSK.
Due to low power consumption of the logic core, no supply buffer capacitor is required. Only an external coil is needed to obtain the chip function. A parallel resonance capacitor of 78 pF is also integrated.

Applications

- Animal implantable transponder
- Animal ear tag
- Industrial transponder

Typical Operating Configuration

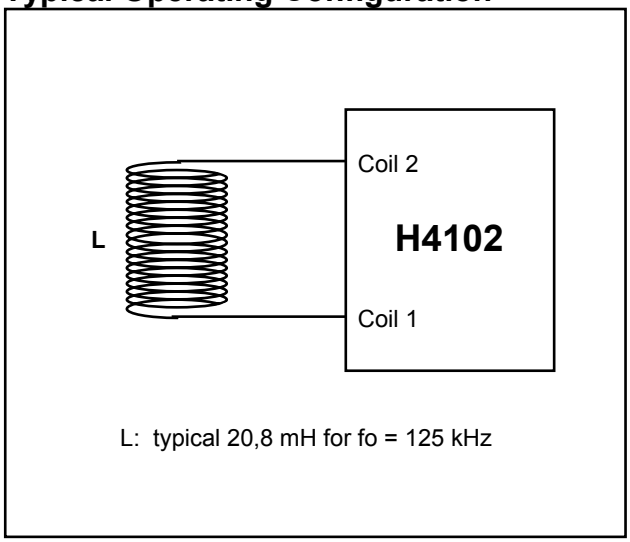

Figure 1

Pin Assignment

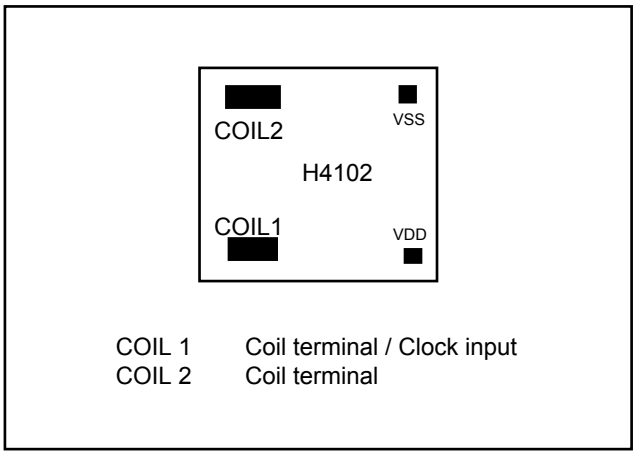

Figure 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum DC Current forced on COIL1 & COIL2	ICOIL	±30mA
Power Supply	VDD	-0.3 to 7.5V
Storage Temp. Die form	Tstore	-55 to +200°C
Storage Temp. PCB form	Tstore	-55 to +125°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	VESD	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device.
Exposure beyond specified operating conditions max affect device reliability or cause malfunction.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Temp.	Top	-40		+85	°C
Maximum Coil Current	ICOIL	-10		10	mA
AC Voltage on Coil	Vcoil	3	14*		Vpp
Supply Frequency	fcoil	100		150	kHz

Table 2

*) The AC Voltage on Coil is limited by the on chip voltage limitation circuitry. This is according to the parameter Icoil in the absolute maximum ratings.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component.

System Principle

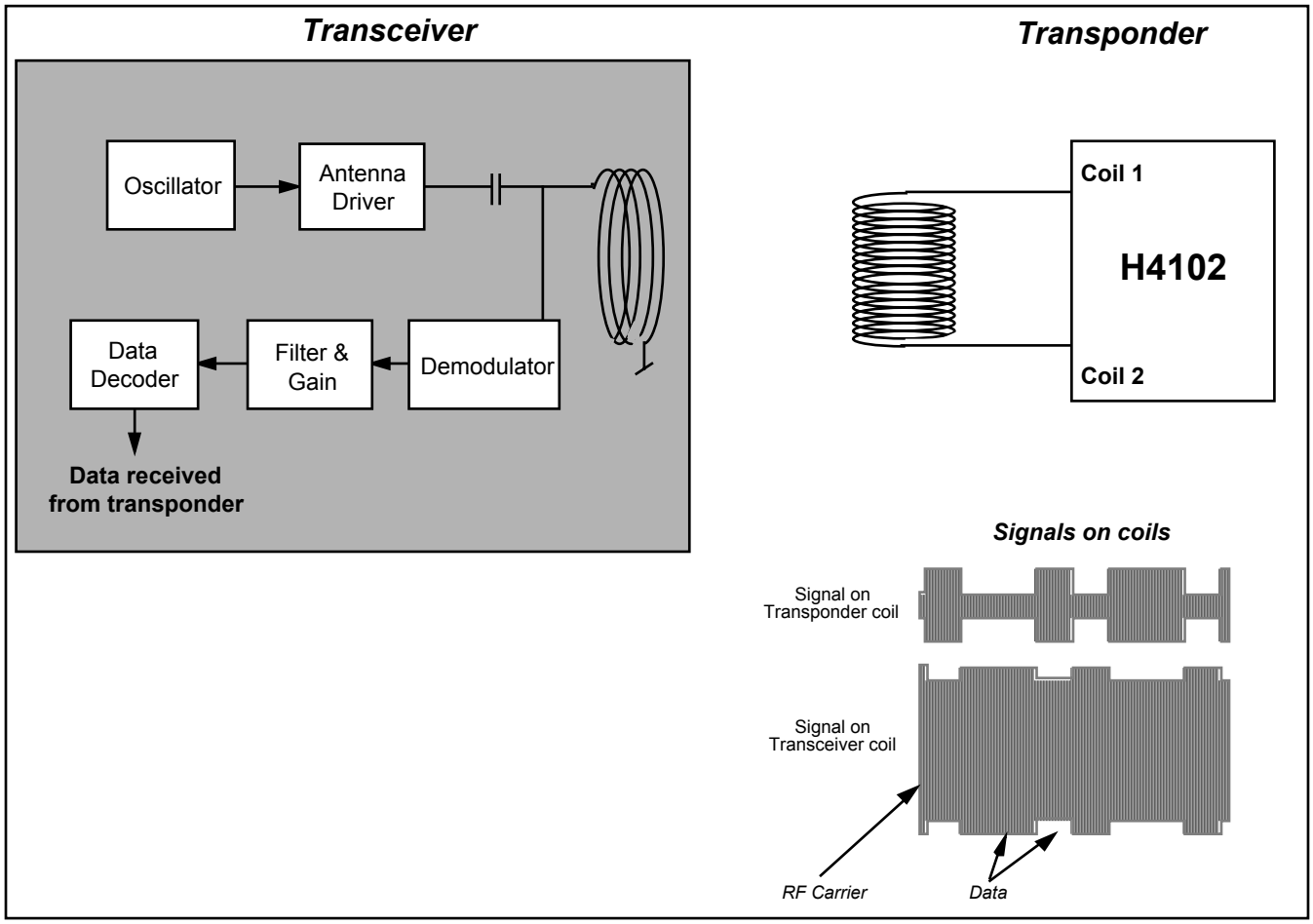

Figure 3

Electrical Characteristics

V_{DD} = 1.5V, V_{SS} = 0V, f_{C1} = 134kHz sine wave, T_a = 25°C
V_{C1} = 1.0V with positive peak at V_{DD} and negative peak at V_{DD} -1V unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		1.5		1)	V
Rectified Supply Voltage	V_{DDREC}	V_{COIL1} - V_{COIL2} = 2.8 VDC Modulator switch = "ON"	1.5			V
Coil1 - Coil2 Capacitance	C_{res}	V_{coil}=100mVRMS f=10kHz		78 2)		pF
Power Supply Capacitor	C_{sup}			125		pF
Manchester and biphase versions						
Supply Current	I_{DD}			0.6	1.5	µA
C2 pad Modulator ON voltage drop	V_{ONC2}	V_{DD}=5.0V I_{VDDC2}=1mA with ref. to V_{DD}	150	220	280	mV
PSK version						
Supply Current	I_{DDPSK}			0.9	2.0	µA
C2 pad Modulator ON voltage drop	$V_{ONC2PSK}$	V_{DD}=5.0V I_{VDDC2}=100µA with ref. to V_{DD}	500	650	800	mV

Table 3

1) The maximum voltage is defined by forcing 10mA on COIL1 - COIL2
2) The tolerance of the resonant capacitor is ± 15% over the whole production.
On a wafer basis, the tolerance is ± 2%

Timing Characteristics

V_{DD} = 1.5V, V_{SS} = 0V, f_{coil} = 134kHz sine wave, T_a = 25°C
V_{C1} = 1.0V with positive peak at V_{DD} and negative peak at V_{DD} -1V unless otherwise specified
Timings are derived from the field frequency and are specified as a number of RF periods.

Parameter	Symbol	Test Conditions	Value	Units
Read Bit Period	T_{rdb}	depending on option	64, 32, 16	RF periods

Table 4

Timing Waveforms

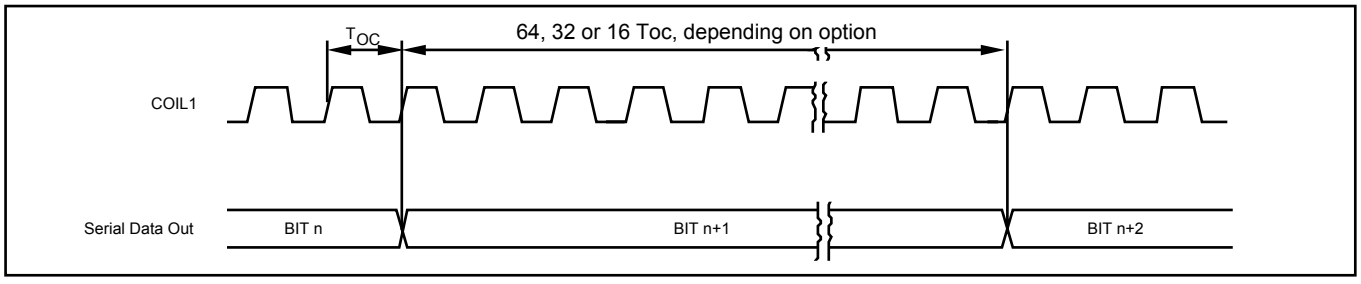

Figure 4

Block Diagram

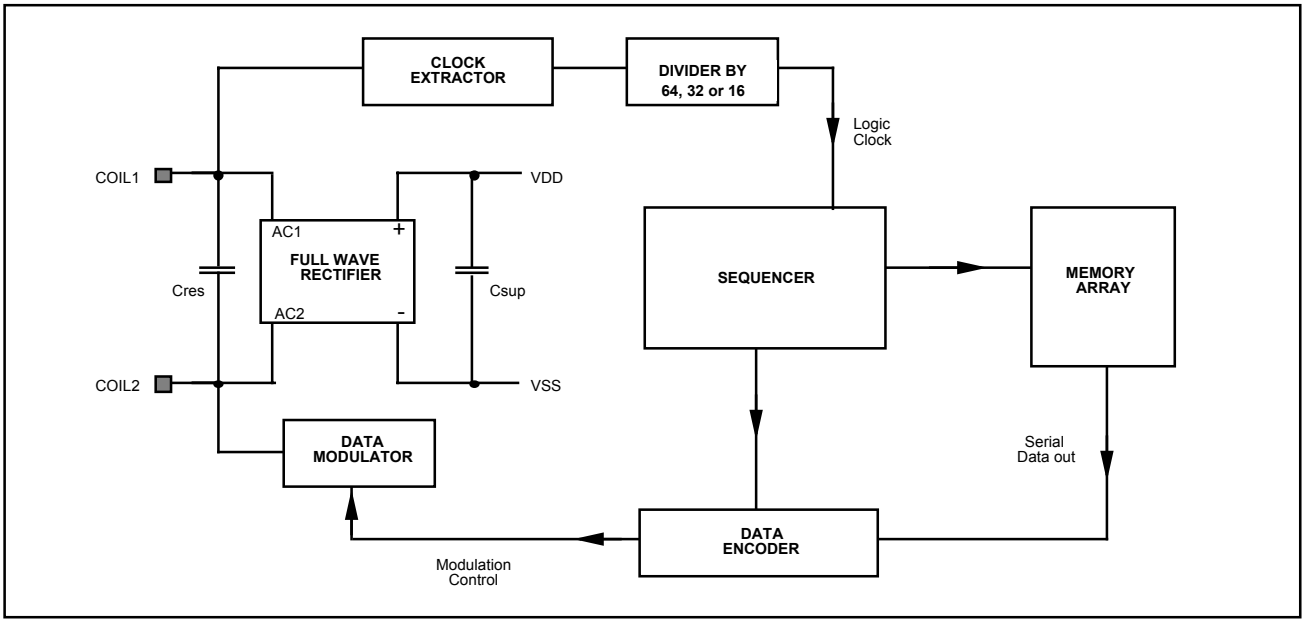

Figure 5

Functional Description

General

The H4102 is supplied by means of an electromagnetic field induced on the attached coil. The AC voltage is rectified in order to provide a DC internal supply voltage. When the last bit is sent, the chip will continue with the first bit until the power goes off.

Full Wave Rectifier

The AC input induced in the external coil by an incident magnetic field is rectified by a Graetz bridge. The bridge will limit the internal DC voltage to avoid malfunction in strong fields.

Clock Extractor

One of the coil terminals (COIL1) is used to generate the master clock for the logic function. The output of the clock extractor drives a sequencer.

Sequencer

The sequencer provides all necessary signals to address the memory array and to encode the serial data out.
Three mask programmed encoding versions of logic are available. These three encoding types are Manchester, biphase and PSK. The bit rate for the first and the second type can be 64 or 32 periods of the field frequency. For the PSK version, the bit rate is 16.

The sequencer receives its clock from the COIL1 clock extractor and generates every internal signal controlling the memory and the data encoder logic.

Data Modulator

The data modulator is controlled by the signal Modulation Control in order to induce a high current in the coil. The coil 2 transistor drives this high current. This will affect the magnetic field according to the data stored in the memory array.

Memory Array for Manchester & Bi-Phase encoding ICs

The H4102 contains 64 bits divided in five groups of information. 9 bits are used for the header, 10 row parity bits (P0-P9), 4 column parity bits (PC0-PC3), 40 data bits (D00-D93), and 1 stop bit set to logic 0.

1	1	1	1	1	1	1	1	1	9 header bits
8 version bits or customer ID				D00	D01	D02	D03	P0	
				D10	D11	D12	D13	P1	
32 data bits				D20	D21	D22	D23	P2	
				D30	D31	D32	D33	P3	
				D40	D41	D42	D43	P4	
				D50	D51	D52	D53	P5	
				D60	D61	D62	D63	P6	
				D70	D71	D72	D73	P7	
				D80	D81	D82	D83	P8	
				D90	D91	D92	D93	P9	10 line parity bits
				PC0	PC1	PC2	PC3	S0	

4 column parity bits

Table 5

The header is composed of the 9 first bits which are all programmed to "1". Due to the data and parity organisation, this sequence cannot be reproduced in the data string. The header is followed by 10 groups of 4 data bits allowing 100 billion combinations and 1 even row parity bit. Then, the last group consists of 4 event column parity bits without row parity bit. S0 is a stop bit which is written to "0"
Bits D00 to D03 and bits D10 to D13 are customer specific identification.
These 64 bits are outputted serially in order to control the modulator. When the 64 bits data string is outputted, the output sequence is repeated continuously until power goes off.

Memory Array for PSK encoding ICs
The PSK coded IC's are programmed with odd parity for P0 and P1 and always with a logic zero.
The parity bits from P2 to P9 are even.
The column parity PC0 to PC3 are calculated including the version bits and are even parity bits.

Code Description

Manchester
There is always a transition from ON to OFF or from OFF to ON in the middle of bit period. At the transition from logic bit “1” to logic bit “0” or logic bit “0” to logic bit “1” the phase change. Value high of data stream presented below modulator switch OFF, low represents switch ON (see Fig. 6).

Biphase Code
At the beginning of each bit, a transition will occur. A logic bit “1” will keep its state for the whole bit duration and a logic bit “0” will show a transition in the middle of the bit duration (see Fig. 7).

PSK Code
Modulation switch goes ON and OFF alternately every period of carrier frequency. When a phase shift occurs, a logical "0" is read from the memory. If no shift phase occurs after a data rate cycle, a logical "1" is read (see Fig. 8).

Manchester Code

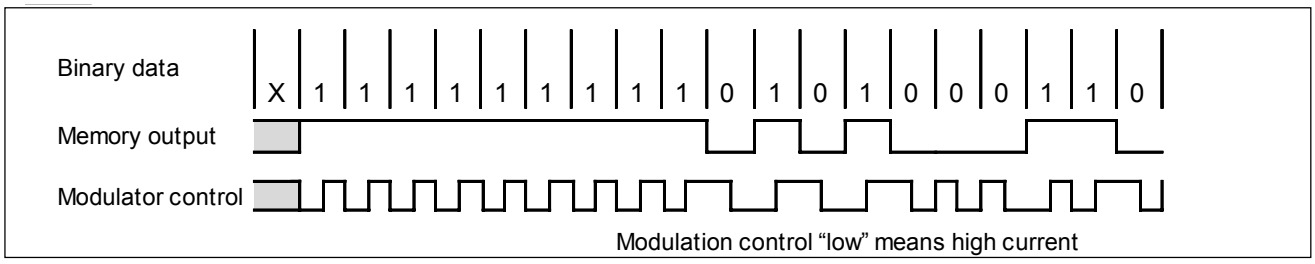

Figure 6

Biphase Code

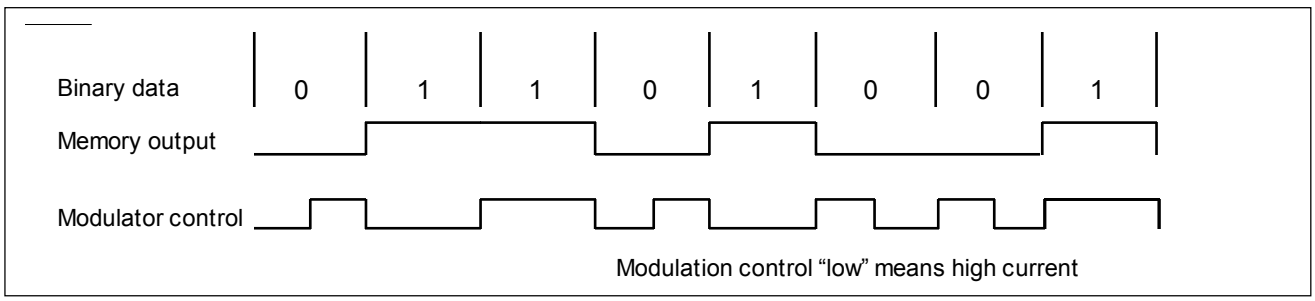

Figure 7

PSK Code

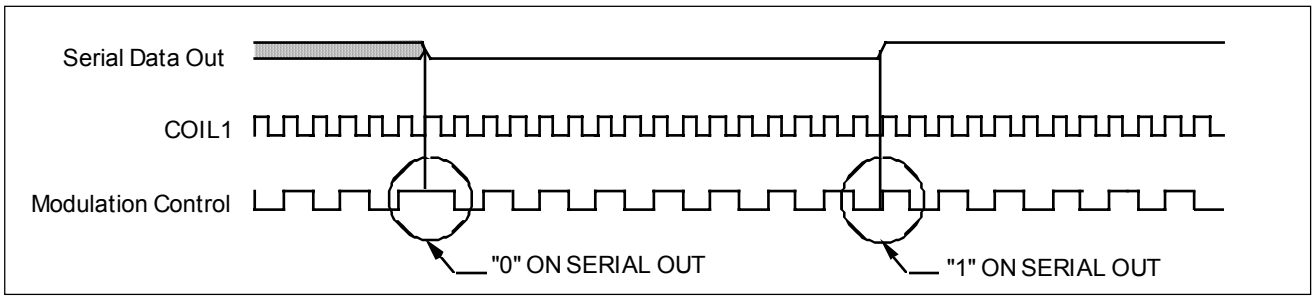

Figure 8

Chip and Ordering Information

CHIP Dimensions

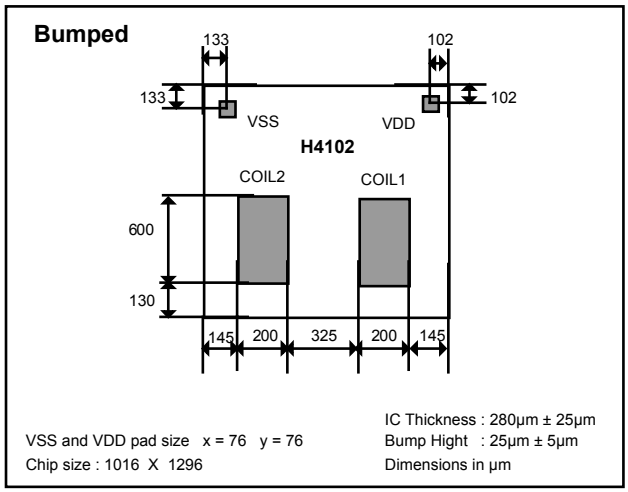

Figure 9

Versions

The following versions are currently available

Versions	Code	Data rate (clocks per bit)
01	Manchester	64
11	Manchester	32
21	Biphase	64
31	Biphase	32
40	PSK	16

Table 6

Ordering Information

The 4102 is available in Chip form with Bumps H4102 <version>